Electronic Version
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Claims

[c1] What is claimed is:

1. An integrated circuit, comprising:

one or more logic stages, at least one of said logic stages having a predominantly high input state or having a predominantly low input state;

wherein said logic stages having said predominantly high input state, comprise one or more thin gate dielectric and high threshold voltage PFETs with respect to a reference PFET and one or more thick gate dielectric and low threshold voltage NFETs with respect to a reference NFET; and

wherein said logic stages having said predominantly low input state, comprise one or more thick gate dielectric and low threshold voltage PFETs with respect to said reference PFET and one or more thin gate dielectric and high threshold voltage NFETs with respect to said reference NFET.

[c2] 2. The circuit of claim 1, wherein:

said logic stages having said predominantly high input state comprise all thin gate dielectric and high threshold voltage PFETs and comprise all thick gate dielectric and

low threshold voltage NFETs; and
said logic stages having said predominantly low input state comprise all thick gate dielectric and low threshold voltage PFETs and comprise all thin gate dielectric and high threshold voltage NFETs.

[c3] 3. The circuit of claim 1, wherein:
all of said logic stages have either a predominantly high input state or a predominantly low input state.

[c4] 4. The circuit of claim 3, wherein logic stages having predominantly high input states are connected in series with logic stages having predominantly low input states, said logic stages having predominantly high input states alternating with logic stages having predominantly low input states.

[c5] 5. The circuit of claim 1, wherein:
said logic stages, further comprise intermediate NFETs or intermediate PFETs or both intermediate NFETs and intermediate PFETs;
wherein for logic stages having said predominantly high inputs, intermediate PFETs are stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs, said intermediate PFETs having a thin gate dielectric with respect to said reference PFET and a threshold

voltage less than the threshold voltage of said thin gate dielectric and high threshold voltage PFET; and
wherein for logic stages having said predominantly low inputs, intermediate NFETs and PFETs are stacked in series between said thick gate dielectric and low threshold voltage PFETs and said thin gate dielectric and high threshold voltage NFETs, said intermediate NFETs having a thin gate dielectric with respect to said reference NFET and a threshold voltages less than that of said high threshold NFET.

[c6] 6. The circuit of claim 1, wherein said logic stages operate monotonically.

[c7] 7. The circuit of claim 1, wherein said logic stages comprise pulsed CMOS logic circuits, dynamic domino circuits or fuse evaluation circuits.

[c8] 8. The circuit of claim 1, wherein said predominantly high input state and said predominantly low input state are independently selected from the group of states consisting of precharge states, standby states, output states of combinational logic coupled to said circuit and output states of previous logic stages of said circuit.

[c9] 9. A method of reducing leakage current in a circuit, comprising:

specifying a reference PFET having a specified threshold voltage and gate dielectric thickness and a reference NFET having a specified threshold voltage and gate dielectric thickness;
providing said circuit, said circuit having one or more logic stages;
connecting at least one of said logic stages to an input having a predominantly high input state or having a predominantly low input state;
wherein said logic stages connected to said input having said predominantly high input state, comprise one or more thin gate dielectric and high threshold voltage PFETs with respect to said reference PFET and one or more thick gate dielectric and low threshold voltage NFETs with respect to said reference NFET; and
wherein said logic stages connected to said input having said predominantly low input state, comprise one or more thick gate dielectric and low threshold voltage PFETs with respect to said reference PFET and one or more thin gate dielectric and high threshold voltage NFETs with respect to said reference NFET.

[c10] 10. The method of claim 9, wherein:
said logic stages having said predominantly high input state comprise all thin gate dielectric and high threshold voltage PFETs and comprise all thick gate dielectric and

low threshold voltage NFETs; and
said logic stages having said predominantly low input state comprise all thick gate dielectric and low threshold voltage PFETs and comprise all thin gate dielectric and high threshold voltage NFETs.

[c11] 11. The method of claim 9, further including connecting all of said logic stages to either said predominantly high input state or said predominantly low input state.

[c12] 12. The method of claim 11, further including connecting logic stages having predominantly high input states in series with logic stages having predominantly low input states, said logic stages having predominantly high input states alternating with logic stages having predominantly low input states.

[c13] 13. The method of claim 9, wherein:
said logic stages, further comprise intermediate NFETs or intermediate PFETs or both intermediate NFETs and intermediate PFETs;
wherein for logic stages having said predominantly high inputs, intermediate PFETs are stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs, said intermediate PFETs having a thin gate dielectric with respect to said reference PFET and a threshold

voltage less than the threshold voltage of said thin gate dielectric and high threshold voltage PFET; and
wherein for logic stages having said predominantly low inputs, intermediate NFETs and PFETs are stacked in series between said thick gate dielectric and low threshold voltage PFETs and said thin gate dielectric and high threshold voltage NFETs, said intermediate NFETs having a thin gate dielectric with respect to said reference NFET and a threshold voltages less that of said high threshold NFET.

[c14] 14. The method of claim 9, further including operating said logic stages monotonically.

[c15] 15. The method of claim 9, wherein said logic stages comprise pulsed CMOS logic circuits, dynamic domino circuits or fuse state evaluation circuits.

[c16] 16. The method of claim 9, wherein said predominantly high input state and said predominantly low input state are independently selected from the group of states consisting of precharge states, standby states, output states of combinational logic coupled to said circuit and output states of previous logic stages of said circuit.

[c17] 17. A method of designing a monotonically operated CMOS circuit having reduced leakage current, compris-

ing:

specifying a reference PFET having a specified threshold voltage and gate dielectric thickness and a reference NFET having a specified threshold voltage and gate dielectric thickness;

defining a CMOS logic circuit having logic stages, said logic stages having input states;

defining a thin gate dielectric and high threshold voltage PFET with respect to said reference PFET, for any of said logic stages having a predominantly high input state;

defining a thick gate dielectric and low threshold voltage NFET with respect to said reference NFET, for any of said logic stages having said predominantly high input state;

defining a thick gate dielectric and low threshold voltage PFET with respect to said reference PFET, for any of said logic stages having a predominantly low input state; and

defining a thin gate dielectric and high threshold voltage NFET with respect to said reference NFET, for any of said logic stages having said predominantly low input state.

[c18] 18. The method of claim 17, further including connecting in series logic stages having predominantly high input states with logic stages having predominantly low input states, said logic stages having predominantly high input states alternating with logic stages having predominantly low input states.

[c19] 19. The method of claim 17, further including:
defining a high intermediate NFET having a thick gate dielectric and a low threshold voltage with respect to said reference NFET for any of said logic stages having said predominantly high inputs, said high intermediate NFET for stacking in series between said thin gate dielectric and high threshold voltage PFET and said thick gate dielectric and low threshold voltage NFET;
defining a high intermediate PFET having a thin gate dielectric with respect to said reference PFET and a threshold voltage less than that of said high threshold voltage PFET for any of said logic stages having said predominantly high inputs, said high intermediate PFET for stacking in series between said thin gate dielectric and high threshold voltage PFET and said thick gate dielectric and low threshold voltage NFET;
defining a low intermediate NFET having a thin gate dielectric with respect to said reference NFET and a threshold voltage less that of said high threshold NFET for any of said logic stages having said predominantly low inputs, said low intermediate NFET for stacking in series between said thin gate dielectric and high threshold voltage PFET and said thick gate dielectric and low threshold voltage NFET; and
defining a low intermediate PFET having a thick gate di-

electric and a low threshold voltage with respect to said reference PFET for any of said logic stages having said predominantly low inputs, said low intermediate PFET for stacking in series between said thin gate dielectric and high threshold voltage PFET and said thick gate dielectric and low threshold voltage NFET.

[c20] 20. The method of claim 17, wherein said logic stages operate monotonically.

[c21] 21. The method of claim 17, wherein said logic stages comprise pulsed CMOS logic circuits, dynamic domino circuits or fuse evaluation circuits.

[c22] 22. The method of claim 17, wherein said predominantly high input state and said predominantly low input state are independently selected from the group of states consisting of precharge states, standby states, output states of combinational logic coupled to said circuit and output states of previous logic stages of said circuit

[c23] 23. A method of designing a monotonically operated CMOS circuit with reduced current leakage, comprising; (a) specifying a reference PFET having a specified threshold voltage and gate dielectric thickness and a reference NFET having a specified threshold voltage and gate dielectric thickness;

(b) synthesizing a schematic circuit design with standard design elements, said standard design elements including one or more reference PFETS and one or more reference NFETs ;

(c) analyzing one or more circuits for logic stages having predominantly high input logic states or predominantly low input logic states;

(d) selecting one or more logic stages determined to have predominantly high input logic states or predominantly low input logic states; and

(e) replacing said standard design elements of said selected logic stages with reduced current leakage elements, said reduced current leakage elements including:

thin gate dielectric and high threshold voltage PFETs with respect to said reference PFET, for logic stages having predominantly high input states;

thick gate dielectric and low threshold voltage NFETs with respect to said reference NFET, for logic stages having predominantly high input states;

thick gate dielectric and low threshold voltage PFETs with respect to said reference PFET, for a logic stages having predominantly low input states; and

thin gate dielectric and high threshold voltage NFETs with respect to said reference NFET, for said logic stages having predominantly low input states.

[c24] 24. The method of claim 23 wherein said reduced current leakage elements further include:
high intermediate NFETs having thick gate dielectrics and low threshold voltages with respect to said reference NFET defined for logic stages having said predominantly high inputs, said high intermediate NFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs;
high intermediate PFETs having thin gate dielectrics with respect to said reference PFET and threshold voltages less than that of said high threshold voltage PFETs defined for logic stages having said predominantly high inputs, said high intermediate PFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs;
low intermediate NFETs having thin gate dielectrics with respect to said reference NFET and threshold voltages less than that of said high threshold NFETs defined for logic stages having said predominantly low inputs, said low intermediate NFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs; and
low intermediate PFETs having thick gate dielectrics and

low threshold voltages with respect to said reference PFET defined for logic stages having said predominantly low inputs, said low intermediate PFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs.

[c25] 25. The method of claim 23, further including:
(f) analyzing the performance of said logic stages with said reduced leakage current elements; and
(g) replacing selected logic stages having been previously replaced with said reduced leakage current elements with reduced current elements further including:
high intermediate NFETs having thick gate dielectrics and low threshold voltages with respect to said reference NFET defined for logic stages having said predominantly high inputs, said high intermediate NFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs;
high intermediate PFETs having thin gate dielectrics with respect to said reference PFET and threshold voltages less than that of said high threshold voltage PFETs defined for logic stages having said predominantly high inputs, said high intermediate PFETs stacked in series between said thin gate dielectric and high threshold volt-

age PFETs and said thick gate dielectric and low threshold voltage NFETs;

low intermediate NFETs having thin gate dielectrics with respect to said reference NFET and threshold voltages less than that of said high threshold NFETs defined for logic stages having said predominantly low inputs, said low intermediate NFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs; and

low intermediate PFETs having thick gate dielectrics and low threshold voltages with respect to said reference PFET defined for logic stages having said predominantly low inputs, said low intermediate PFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs.

[c26] 26. The method of claim 23, wherein all PFETs of said reduced leakage current elements are selected from the group of PFETs consisting of thin gate dielectric and high threshold voltage PFETs for logic stages having predominantly high input states and thick gate dielectric and low threshold voltage PFETs for logic stages having predominantly low input states; and

wherein all NFETs of said reduced leakage current ele-

ments are selected from the group of NFETs consisting of thick gate dielectric and low threshold voltage NFETs for logic stages having predominantly high input states and thin gate dielectric and high threshold voltage NFETs for said logic stages having predominantly low input states.

[c27] 27. The method of claim 23, wherein said predominantly high input state and said predominantly low input state are independently selected from the group of states consisting of precharge states, standby states, output states of combinational logic coupled to said circuit and output states of logic stages of said circuit.

[c28] 28. A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method for designing a monotonic CMOS circuit with reduced current leakage, said method comprising the computer implemented steps of:

(a) specifying a reference PFET having a specified threshold voltage and gate dielectric thickness and a reference NFET having a specified threshold voltage and gate dielectric thickness;

(b) synthesizing a schematic circuit design with standard

design elements, said standard design elements including one or more reference PFETS and one or more reference NFETs;

(c) analyzing one or more circuits for logic stages having predominantly high input logic states or predominantly low input logic states;

(d) selecting one or more logic stages determined to have predominantly high input logic states or predominantly low input logic states; and

(e) replacing said standard design elements of said selected logic stages with reduced current leakage elements, said reduced current leakage elements including:

thin gate dielectric and high threshold voltage PFETs with respect to said reference PFET, for logic stages having predominantly high input states;

thick gate dielectric and low threshold voltage NFETs with respect to said reference NFET, for logic stages having predominantly high input states;

thick gate dielectric and low threshold voltage PFETs with respect to said reference PFET, for a logic stages having predominantly low input states; and

thin gate dielectric and high threshold voltage NFETs with respect to said reference NFET, for said logic stages having predominantly low input states.

[c29] 29. The method of claim 28 wherein said reduced cur-

rent leakage elements further include:

high intermediate NFETs having thick gate dielectrics and low threshold voltages with respect to said reference NFET defined for logic stages having said predominantly high inputs, said high intermediate NFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs;

high intermediate PFETs having thin gate dielectrics with respect to said reference PFET and threshold voltages less than that of said high threshold voltage PFETs defined for logic stages having said predominantly high inputs, said high intermediate PFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs;

low intermediate NFETs having thin gate dielectrics with respect to said reference NFET and threshold voltages less than that of said high threshold NFETs defined for logic stages having said predominantly low inputs, said low intermediate NFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs; and

low intermediate PFETs having thick gate dielectrics and low threshold voltages with respect to said reference

PFET defined for logic stages having said predominantly low inputs, said low intermediate PFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs.

[c30] 30. The method of claim 28, further including:
(f) analyzing the performance of said logic stages with said reduced leakage current elements; and
(g) replacing selected logic stages having been previously replaced with said reduced leakage current elements with reduced current elements further including:
high intermediate NFETs having thick gate dielectrics and low threshold voltages with respect to said reference NFET defined for logic stages having said predominantly high inputs, said high intermediate NFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs;
high intermediate PFETs having thin gate dielectrics with respect to said reference PFET and threshold voltages less than that of said high threshold voltage PFETs defined for logic stages having said predominantly high inputs, said high intermediate PFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low thresh-

old voltage NFETs;

low intermediate NFETs having thin gate dielectrics with respect to said reference NFET and threshold voltages less than that of said high threshold NFETs defined for logic stages having said predominantly low inputs, said low intermediate NFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs; and

low intermediate PFETs having thick gate dielectrics and low threshold voltages with respect to said reference PFET defined for logic stages having said predominantly low inputs, said low intermediate PFETs stacked in series between said thin gate dielectric and high threshold voltage PFETs and said thick gate dielectric and low threshold voltage NFETs.

[c31] 31. The method of claim 28, wherein all PFETs of said reduced leakage current elements are selected from the group of PFETs consisting of thin gate dielectric and high threshold voltage PFETs for logic stages having predominantly high input states and thick gate dielectric and low threshold voltage PFETs for a logic stages having predominantly low input states; and

wherein all NFETs of said reduced leakage current elements are selected from the group of NFETs consisting

of thick gate dielectric and low threshold voltage NFETs for logic stages having predominantly high input states and thin gate dielectric and high threshold voltage NFETs for said logic stages having predominantly low input states.

[c32] 32. The method of claim 28, wherein said predominantly high input state and said predominantly low input state are independently selected from the group of states consisting of precharge states, standby states, output states of combinational logic coupled to said circuit and output states of logic stages of said circuit.